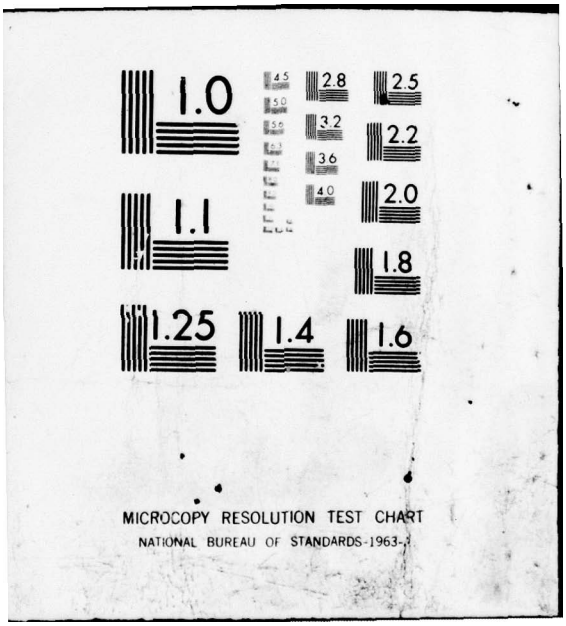
AD-A074 721 YUCCA INTERNATIONAL INC SCOTTSCALE AZ F/G 9/2
MICROPROCESSOR EVALUATION. ITEM 0003 OF MICROPROCESSOR-BASED PO--ETC(U)
NOV 78 DAAK70-78-C-0117
UNCLASSIFIED NL

1 OF 1
AD A074 721

END
DATE FILMED
11-78
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

LEVEL II

MICROPROCESSOR EVALUATION

ITEM 0003

OF

MICROPROCESSOR-BASED POWER CONDITIONER CONTROLLER

CONTRACT NO. DAAK70-78-C-0117

PREPARED FOR

U. S. ARMY MERADCOM

FORT BELVOIR, VIRGINIA 22060

(11) Nov 78

(12) 29

PREPARED BY

YUCCA INTERNATIONAL INCORPORATED

14415 N. SCOTTSDALE ROAD

SUITE 700

SCOTTSDALE, ARIZONA 85260

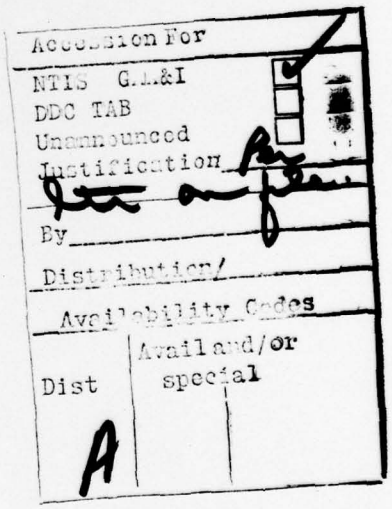
392 729

NOVEMBER 1978

392 729

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS



1.0.0 SUMMARY

This report covers effort under contract DAAK70-78-C-0117 to develop a microprocessor-based controller for the Delco 15 KW power conditioner.

Continuing, from the controller baseline design, the previous task, the selection of the optimum microprocessor was performed.

The selection was made from all of the microprocessors known to Yucca at the beginning of this task. The microprocessors were quickly eliminated down to eight with elimination criteria developed and listed in this report. Next, an evaluation of the remaining microprocessors was made and a trade-off study of the three best microprocessors was performed. These were the 8085A-2, the Z80A, and the MC68B09. The latter offered the best compromise of many key features which included low minimum system chip count and power consumption.

The MC68B09 is the optimum microprocessor capable of performing the duties required in the microprocessor-based controller and is both flexible and expandable to accomodate modifications during development.

2.0.0 PREFACE

The work described in this report was performed by Yucca International, Inc. under the direction of the U. S. Army Mobility Equipment Research and Development Command. This report completes the third task of the first phase (CLIN 0003, Phase 1) of the U. S. Army contract no. DAAK70-78-C-0117. The Contracting Officer's Representative is Dr. David Lee at the U. S. Army MERADCOM Headquarters at Fort Belvoir, Virginia.

3.0.0 COPYRIGHT PERMISSION

The information contained in this report was derived from commonly available microprocessor data sheets and user manuals. Figure 4 in this report was obtained from an MC6809 Advanced Microprocessor Manual. No copyright permission is required.

4.0.0 INTRODUCTION

This is a report of the third task of six tasks of the U. S. Army contract no. DAAK70-78-C-0117.

Performed during the previous tasks was the baseline design of a microprocessor-based controller for the Delco 15 KW power conditioner to replace an existing controller. During this task, an optimum microprocessor for the controller will be selected.

The microprocessor to be selected should perform efficiently, any task expected of the microprocessor. Other factors that will influence the selection are overall system complexity, ease of programming, flexible instruction set and system expansion capability.

Many microprocessors are available to select from. Some are obsolete and some are special purpose devices not ideally suited for the controller. Microprocessors differ in speed, instruction set efficiency and flexibility, power consumption, expandability and additional features. This is because CMOS, PMOS, NMOS, and bi-polar microprocessors may be available in single bit, bit-slice, 4 bit, 8 bit, or 16 bit architectures. Also, microprocessors have been developed to execute inferior instruction sets used previously by minicomputers because a large amount

of software is available. To justify why a microprocessor can be eliminated from possible selection, some specific requirements of the application must be known.

The first part of this report concerns the derivation of criteria to be used for narrowing the possible selection from all microprocessors known to Yucca to only eight.

The selection will be further narrowed to three microprocessors. A trade-off study will be performed to select the optimum microprocessor.

5.0.0 INVESTIGATION

5.1.0 MICROPROCESSOR INPUT/OUTPUT REQUIREMENTS

Figure #1 shows how 21 I/O lines can be designated to control the controller modules. Also shown are the three interrupts.

The power supply failure interrupt will require a non-maskable interrupt (this is an interrupt which cannot be disabled). The microprocessor upon receiving a power supply failure interrupt will deactivate the power conditioner before the microprocessor power supply drops below a critical level.

The converter operating cycle interrupt will measure the converter output voltage and make a correction to the converter operating frequency if necessary. This interrupt will be maskable by the microprocessor.

The commutation fail interrupt will also be a maskable interrupt.

Figure #1 includes two signal lines labeled slow fan speed and overtemperature. These will require either 2 I/O lines or two interrupt lines. The microprocessor that is selected will form part of a minimum system. This system should include enough I/O to accomodate the signals in Figure #1. Capability for I/O expansion should also be provided to meet future needs.

5.2.0 MICROPROCESSOR ADDRESS AND DATA BUS REQUIREMENTS

Figure #2 shows how the address lines and data bus of the selected microprocessor can be used to generate the necessary read data and write data strobe signals. These will be used to enable write data and read data to and from the controller modules. A common 8 bit data bus or separated 8 bit read bus and write bus will transfer data between the microprocessor data bus and the controller modules.

The selected microprocessor will have all address lines and data lines available to permit memory expansion, I/O expansion, and additional peripherals if necessary.

5.3.0 ELIMINATION CRITERIA AND ADDITIONAL MICROPROCESSOR REQUIREMENTS

The power conditioner controller is not expected to impose any speed requirements or power requirements that will automatically mandate a bi-polar or CMOS microprocessor, respectively. Microprocessors will be eliminated from possible selection for the following reasons:

1) Microprocessors which will not directly address more than 4K bytes will be eliminated. The microprocessor should be capable of supporting software and hardware expansion if it becomes necessary. Hardware expansion is simpler if ample address lines are available.

2) Microprocessors that require multiple power supplies will be eliminated. Many of the newer microprocessors offer single supply operation. It will eliminate the need for additional filtering on existing power supplies, and also, simplify power supply failure detection circuitry.

3) Microprocessors which are not TTL compatible will be eliminated.

4) Microprocessors which will not support multiprocessor configurations will be eliminated. Multiprocessor capability will be reserved to increase design flexibility. The microprocessor must have DMA capability.

5) The microprocessor will be required to execute programs which will perform 16 bit arithmetic and 8 bit multiplication and division with 16 bit results. These programs will utilize shift and rotate instructions extensively. The ability to perform arithmetic operations and to move data efficiently will be an important factor in the selection.

6) Microprocessors which will execute the PDP-8, Nova, or F-8 instruction set will be eliminated. It is Yucca's opinion that these instruction sets are inferior to other instruction sets available in many other microprocessors.

7) Bit slice, bi-polar, or PMOS microprocessors will be not be considered for selection. NMOS or CMOS will be selected. Bit slice arithmetic logic units require higher component counts, higher development costs, and perhaps higher power requirements. Bi-polar offers high speed at the expense of power consumption. NMOS is a suitable compromise of speed vs. power consumption. PMOS is slower than NMOS and is not being used in the newer microprocessors.

8) The newest microprocessors may be eliminated from selection due to unavailability.

9) Microprocessors will be eliminated if it is doubtful that the part will be MIL qualified or second-sourced.

10) Microprocessors which are not supported with a prototyping kit and a development system will be eliminated. Ample development tools will speed development and debug of software and hardware.

11) Microprocessors which do not have a non-maskable interrupt will be eliminated.

12) Microprocessors having a data bus less than 8 bits wide will be eliminated.

5.4.0 MICROPROCESSOR ELIMINATION

The microprocessors which were considered for selection but eliminated for the reasons listed in section 5.3.0 are listed below:

Microprocessor	Reason Number	Comments
Data General MN601	2, 6, 10	4 supplies
Fairchild 3850 (F-8)	2, 6	2 supplies
General Instrument CP1600/1610	2	3 supplies
Intel 8080A	2	3 supplies
Intel 8021	1	
Intel 8035	1	
Intel 8039	1	
Intel 8048	1	
Intel 8748	1	
Intel 8049	1	

Microprocessor	Reason Number	Comments
Intersil 6100	1, 6	
Mostek 3872	1, 6	
Motorola MC14500	12	
Motorola MC68000	8	
National Semiconductor 1N58060	1, 2	
National Semiconductor 1N58900	2, 3	3 supplies
Panafcom MN1610	2, 10	3 supplies
Texas Instruments TMS9900	2, 10	3 supplies
Texas Instruments TMS9940	1	
Texas Instruments TMS9985	8	Availability date 3/79
Western DIgital WD-16	2	
Zilog Z8	8	Availability date 1st quarter 1979
Zilog Z8000	8	Availability date 1st quarter 1979

Listed below are other microprocessors which were also eliminated.

The Signetics 2650 has a primitive stack. The stack will only hold 8 addresses. It does not have a non-maskable interrupt. It does not have an on-chip clock oscillator. Although it has many addressing modes and other good features, it cannot be considered as an optimum microprocessor candidate.

The Motorola 6800 will be eliminated because of the availability of several microprocessors which are 6800 upgrades. These are the 6801, 6802, and 6803. Of these, the 6801 and 6803 will be retained for further evaluation because of their enhanced instruction sets.

MOS Technology has a broad line of microprocessors. The MCS-6502 offers an on-board clock oscillator and 64K addressing capability. It will be retained as an optimum microprocessor candidate.

The microprocessor elimination leaves the eight remaining candidates listed below:

Intel 8085A-2

Intel 8086

Motorola MC6801

Motorola MC6803

Motorola MC68B09

MOS Technology MCS-6502

RCA 1802

Zilog Z80A

5.5.0 EVALUATION OF EIGHT CANDIDATES

5.5.1 RCA 1802

Advantages

a) CMOS - high noise immunity, military temperatures, low power consumption.

Disadvantages

a) Relatively difficult to program;

b) Addressing modes, interrupt handling, and instruction execution time are inferior to those of other microprocessors;

c) The instruction set is not suited to mathematical manipulations;

d) The single status flag (DF) makes signed arithmetic very difficult;

e) The clock must be externally generated;

f) The eight address lines are multiplexed. This will necessitate demultiplexing logic;

g) The RCA 1802 does not have a non-maskable interrupt.

Due to the disadvantages listed above, the RCA 1802 was eliminated.

5.5.2 MOS TECHNOLOGY MSC-6502

Advantages

a) Enhancement of MC6800 (incompatible);

b) Has built-in clock logic;

c) Has direct addressing, indexed addressing, and indirect addressing;

d) Has based page index addressing;

e) Has a non-maskable interrupt.

Disadvantages

a) The stack is limited to 256 bytes;

b) Stack must be assigned to addresses 0100H to 01FFH;

c) The MCS-6502, like the 6800, does not have a fast interrupt; The interrupt automatically saves all the registers which can be useful but will take unnecessary excess time if this capability is not needed.

Due to the disadvantages listed above, and the fact that many of the desirable features contained in the MCS-6502 are available in the Motorola 68B09, this device was eliminated.

5.5.3 INTEL 8086

Advantages

This microprocessor is the only 16 bit microprocessor of the 8 candidates and for the following reasons, it is the most powerful.

a) It will perform 8 and 16 bit signed and unsigned arithmetic in binary and decimal including multiply or divide;

b) The 8086 will directly address 1 megabyte of memory;

c) The 8086 will support the following software disciplines;

   1) position-independent code; intrasegment calls and jumps specify a relative displacement from the program counter;

   2) Re-entrant programs; a routine usable by interrupt and non-interrupt programs without loosing data;

   3) Dynamically relocatable programs; programs can be relocated in memory and executed by changing the contents of segment registers.

Intel claims that the 8086 has "powerful register structure, unlimited levels of interrupts, powerful input and output circuitry, improved bit manipulation, interruptible byte string operations, very flexible memory addressing, high computational throughput."

From review of the instruction set and previous development experience with this product, these claims are not challenged by Yucca. It is a very powerful microprocessor, but, for reasons to be presented, it is unsuitable for the controller.

A minimum system will consist of the following:

QUANTITY	NAME	DESCRIPTION	CURRENT PER DEVICE	TOTAL CURRENT
1	8086	CPU	275 ma	275 ma
1	8284	Clock Generator	140 ma	140 ma
2	8282	Octal latch	160 ma	320 ma
2	8286	Tranceiver	135 ma	270 ma
4	2142	1K X 4 Bit RAM	100 ma	400 ma
2	2716-2	PROMS	100 ma	200 ma
1	8255	Parallel Peripheral Interface	120 ma	120 ma

A wait-state generator will probably be needed. An additional 8282 will be required to extend addressing from 64K to 1 megabyte. A timer/counter is not included. Total current demand for the minimum system on the +5 volt power supply will be 1.725 amps. The 8086 minimum system chip count and total current is very high when compared to that obtainable with the Z80A, 8085A-2, or the 68B09.

The 8086 is eliminated because a better compromise between computational power, chip count, and power consumption can be found in the remaining candidates.

5.5.4 MOTOROLA MC6801, MC6803

The MC6801 and MC6803 are new single chip microcomputers that will be available soon. They offer identical enhanced versions of the MC6800 instruction set. The instruction set enhancements include 16 bit arithmetic (load, store, add, subtract) and 16 bit logical shift instructions. Also included is an 8 bit X 8 bit unsigned multiply instruction and other instructions.

The MC6801 will have 2K bytes of ROM, 128 bytes of RAM, UART, 31 I/O lines and a 16 bit timer/counter. The MC6801 can use 16 I/O lines to address external memory. Eight of these lines will form the upper 8 bits of the address and the lower 8 lines will multiplex the least significant address lines with data.

THe MC6803 will have 128 bytes of RAM, a UART, 16 bit timer/counter and 13 bi-directional I/O lines.

These will be eliminated from the selection because the MC68B09 has superior addressing modes, interrupt handling capability, and has an instruction cycle time of 1 μs. The MC6801 and MC6803 instruction cycle times will be 2 μs.

5.5.5 INTEL 8085A-2

Advantages

a) 8080A enhancement and software compatible;

b) Non-maskable interrupt;

c) 3 maskable levels of hardware vectored interrupts;

d) serial input and output capability;

e) Instruction set identical to 8080A, except two instructions added to support hardware interrupts and serial capability;

f) A low priority, maskable, general purpose interrupt is available which will permit an interrupt to be vectored anywhere in memory;

g) Register oriented architecture permits fast, arithmetic operations and register move operations (Usually in one instruction cycle if data is already in a register).

h) Instruction cycle (fetch opcode and execute) is .8 μs;

i) Directly addresses 64K bytes of memory and 256 bytes of I/O;

j) Minimum system can be implemented with three chips: 8085A-2, 8355, 8156. Total current is 530 ma. These chips offer 2K X 8 ROM, 256 X 8 RAM, 38 programmable I/O lines, and 14 bit counter/timer;

k) Clock logic is on the chip;

l) Second sources are Siemans and Advanced Micro Devices;

m) Military operating temperatures are expected;

n) Efficient stack operations.

Disadvantages

a) The data bus is multiplexed with the low order address lines. Memory expansion will require an octal latch for demultiplexing the bus;

b) The 8085A-2 has no program counter relative addressing, therefore, all jumps and calls require a 16 bit (2 byte) absolute address. 8 bit relative addressing is preferred because it allows a program to require less memory and address fetch time;

c) Rotate and shift instructions are very useful in performing division and multiplication. The 8085A-2 can rotate or shift the accumulator only. If several bytes must be rotated or shifted, then each byte must be moved to the accumulator and move back again. (The 6809 can rotate or shift the accumulator or any RAM memory location.)

d) The 8085A-2 memory reference instruction utilizes two byte absolute addressing only. One byte direct addressing can reduce the memory requirements of a program.

5.5.6 ZILOG Z80A

Advantages

a) 8080A enhancement. 8080A instruction set is a subset of the Z80A instruction set;

b) Non-maskable interrupts;

c) A maskable general purpose interrupt and an interrupt acknowledge signal permits the interrupt to be vectored to any memory location;

d) The Z80A contains 80 more instructions than the 8080A;

e) The Z80A has two sets of 8080A registers. Single level interrupts are easily handled by switching to the alternate register set instead of saving the registers on a stack;

f) Two index registers are available to facilitate indexed memory addressing with some instructions;

g) In addition to the 8080 and 8085 addressing modes, the Z80A has; one byte relative addressing (which can reduce memory requirement), and bit addressing. The Z80A can set, reset, and test any bit in any memory location or CPU register with one instruction;

h) One byte direct addressing is permitted to only eight locations in page zero (0000H - 00FFH);

i) Built-in dynamic RAM refresh circuitry;

j) instruction cycle time is 1 μs;

k) Directly addresses 64K bytes of memory and 256 bytes of I/O;

l) Second source is Mostek;

m) Military operating temperatures are expected;

n) A minimum system can be constructed with the following:

QTY			
1	Z80A	4.5 MHz CPU	90 ma
1	MK34000	2K X 8 ROM	60 ma
2	MK3881	Parallel I/O Controller	150 ma X 2 = 300 ma
1	MK3886	Z80 Combo Chip	180 ma (estimate based on Intel 8156)
1	Clock Oscillator		100 ma (estimate based on Motorola MC6870)

The MK3881 has 16 bi-directional I/O lines. At least 21 I/O lines are needed for the controller, therefore, 2 MK3881 packages are required.

Samples of the MK3886 will be available 4th quarter 1978. It will have 256 X 8 bytes of RAM, two programmable timers, serial I/O port and interrupt handling circuitry.

Total estimated current is 730 ma.

Disadvantages

a) Most of the 80 new instructions require an additional byte to specify the instruction. This increases memory requirements and increases the number of instruction cycles to accomplish the operation.

b) The Z80A requires an external clock oscillator.

Additional comments:

The 8080A only had 12 unused instruction codes. The Z80A uses 5 of these codes for jumping conditionally and unconditionally to a memory location relative to the program counter. The maximum displacement is ± 128 bytes. Three opcodes are used for other instructions. The four remaining opcodes are used to indicate that an additional byte of opcode follows to specify a new Z80A instruction.

This points out the fact that additional instructions have been added without the need for two bytes of opcode.

5.5.7 MOTOROLA MC68B09

The MC68B09 is a 2MHz version of the MC6809 which operates at 1MHz.

Advantages

a) Psuedo 16 bit microprocessor;
b) 16 bit arithmetic operations (load, store, add, subtract, and compare);
c) 8 bit X 8 bit unsigned multiply instruction;
d) Non-maskable interrupt (NMI) is vectored;
e) Fast interrupt request (FIRQ) is maskable and vectored;
f) Low priority general purpose interrupt (IRQ) is vectored. If it is desired, the vector ROM may be disabled by the user with the aid of the interrupt acknowledge signal. This allows the user to divert the vector from the address programmed in the vector ROM to any memory location;

g) The instruction set includes three software interrupts. Each will save all of the CPU registers and vector to an address contained in a ROM vector location;

h) Built-in clock is optional;

i) Instruction cycle time is 1 μs;

j) Directly addresses 64K bytes of memory;

k) Minimum system can be implemented with four chips: 68B09, 68B10, 68B46, 68B21. Total current is 660 ma. These chips offer 2K bytes ROM, 128 bytes RAM, 16 bit timer/counter and 24 bi-directional I/O lines.

Note: The 6846 will be available 1st quarter 1979.

l) Second source is expected. It will probably be Fairchild. Motorola and Fairchild have a mask exchange agreement;

m) Military operating temperatures are expected.

Disadvantages

a) The 68B09 does not have bit addressing capability (The Z80A does);

b) The 68B09, unlike the 6801 and 6803 does not have 16 bit logical shift capability. This could be particularly useful in division and multiplication routines. It does have 8 bit logical and arithmetic rotate and shift instructions that can be combined to perform a 16 bit logical shift, but two instructions are required instead of one.

Aditional comments

The MC68B09 has 19 addressing modes, 13 more than the MC6800.

The 68B09 permits direct addressing to page zero (0000H - 00FFH). A direct page register can be changed to divert direct addressing to any page. Direct addressing applies to all memory access instructions.

The 68B09 permits byte and 16 bit PC relative addressing.

The 68B09 has 4 indexable registers (2 index registers and 2 stack pointers with index capability) with 8 or 16 bit offset capability. Automatic increment and decrement is included. Indexed addressing capability applies to all memory access instructions.

Indirect addressing modes include: Indexed indirect, indexed immediate offset indirect, indexed register offset indirect, indexed indirect post-increment, pre-decrement indexed indirect. Any of the four indexable registers may be used in the above indexed operations.

The MC68B09 stack operations include: Push and pull on 2 stacks, push and pull any number of registers, index registers may be stack pointers.

The MC68B09 will support multiprocessor operations with the following hardware control signals: Processor busy, memory ready, bus available.

Motorola states the MC68B09 will support the following software disciplines:

a) Position-independent code, due to 16 bit relative addressing capability, a program can execute properly anywhere in the address space;

b) Re-entrant programs; routine useable by interrupt and non-interrupt programs without loosing data;

c) Multi-task and multi-processor organization.

5.6.0 TRADE OFF STUDY

This section will compare the features of the Z80A, 8085A-2, and the 68B09.

Minimum System Complexity

Figure 3 indicates that the Z80A minimum system is more complex than the others. The 8085A-2 minimum system uses slightly less current and provides more RAM and I/O than the 68B09 minimum system.

Addressing Modes

The addressing modes of the 68B09 are superior to those of the Z80A or 8085A-2. The 68B09 has 19 modes, the Z80A has 10 modes, the 8085A-2 has four modes.

Memory Requirements

Due to the flexible addressing modes of the 68B09, less memory will be required to contain a program if compared to the memory required by the other two microprocessors. Many Z80A instructions require two bytes of opcode. Z80A direct addressing is limited to eight locations on page zero. The 8085A-2 has no one byte relative addressing or one byte direct addressing.

Bit Addressing

Unfortunately, bit addressing (provided by Z80A) is not one of the 68B09 addressing modes. This would be useful for addressing individual I/O lines to the controller modules, but it is not a critical requirement.

Interrupt Features

The interrupt features of the 68B09 are preferred over those available from the other two microprocessors. The 68B09 has three software interrupts that can be useful in addition to the other vectored interrupts that are provided.

Multiplication

The 68B09 can multiply two unsigned 8 bit binary numbers with a single instruction and give a 16 bit result. This instruction will execute in 11 μs. This instruction cannot be found in the 8085A-2 or the Z80A. To accomplish the same result, many individual instructions will be required which will use more memory and take more time.

Division

The 68B09 will perform 16 bit arithmetic. These operations are (load, store, add, subtract, and compare). These instructions can be very useful in performing 8 bit X 8 bit binary division. The 8085A-2 and Z80A can perform some limited 16 bit operations.

Benchmark testing

Shown in Figure 4 are the results of benchmark testing performed by Motorola. This is intended to indicate that the 68B09 performs very well overall when compared to the 8085A and the Z80A.

The MC68B09 is the optimum microprocessor recommended by Yucca International, Inc. for the microprocessor-based power conditioner controller.

6.0.0 DISCUSSION

During the course of this microprocessor selection, prime importance has been placed in minimizing power supply circuitry, number of components required for the minimum system, memory requirements, and power consumption. A microprocessor was selected that did not sacrifice performance or flexibility to accomplish this. Flexibility and memory expansion capability could be needed if modifications are necessary as controller development progresses. Consideration was not only given for possible future expansion, but also for possible future minimization of the controller hardware.

If memory requirements can be kept below certain levels during the course of the development, it may be possible to drop down from the 6809 4 chip minimum system to a single chip microcomputer once the design is semi-finalized. The Motorola 6801 and 6803 could be likely candidates for this.

Development of the 68B09 based controller can be performed using the Exorciser, a Motorola development system already at Yucca.

Additional development support can be obtained by purchasing an MC6809 simulator, and MC6809 macro assembler and related reference manuals.

The MC6809 will be available in December 1978. Motorola has stated in a recent seminar that the single unit quantity price of an industrial grade MC6809 will be $19.95.

7.0.0 CONCLUSIONS

The optimum microprocessor for the microprocessor-based controller is the Motorola MC68B09.

It offers the best compromise of performance, complexity of a minimum system, expansion capability, and power supply requirements of all the microprocessors that were considered for selection.

Sufficient development support exists so that development of the 6809 based system may proceed immediately.

8.0.0 RECOMMENDATIONS

It is recommended that Yucca International proceed immediately to the next task, development of the controller hardware.

9.0.0 DISTRIBUTION

Three copies - Dr. W. David Lee

Two copies - John A. Gabby

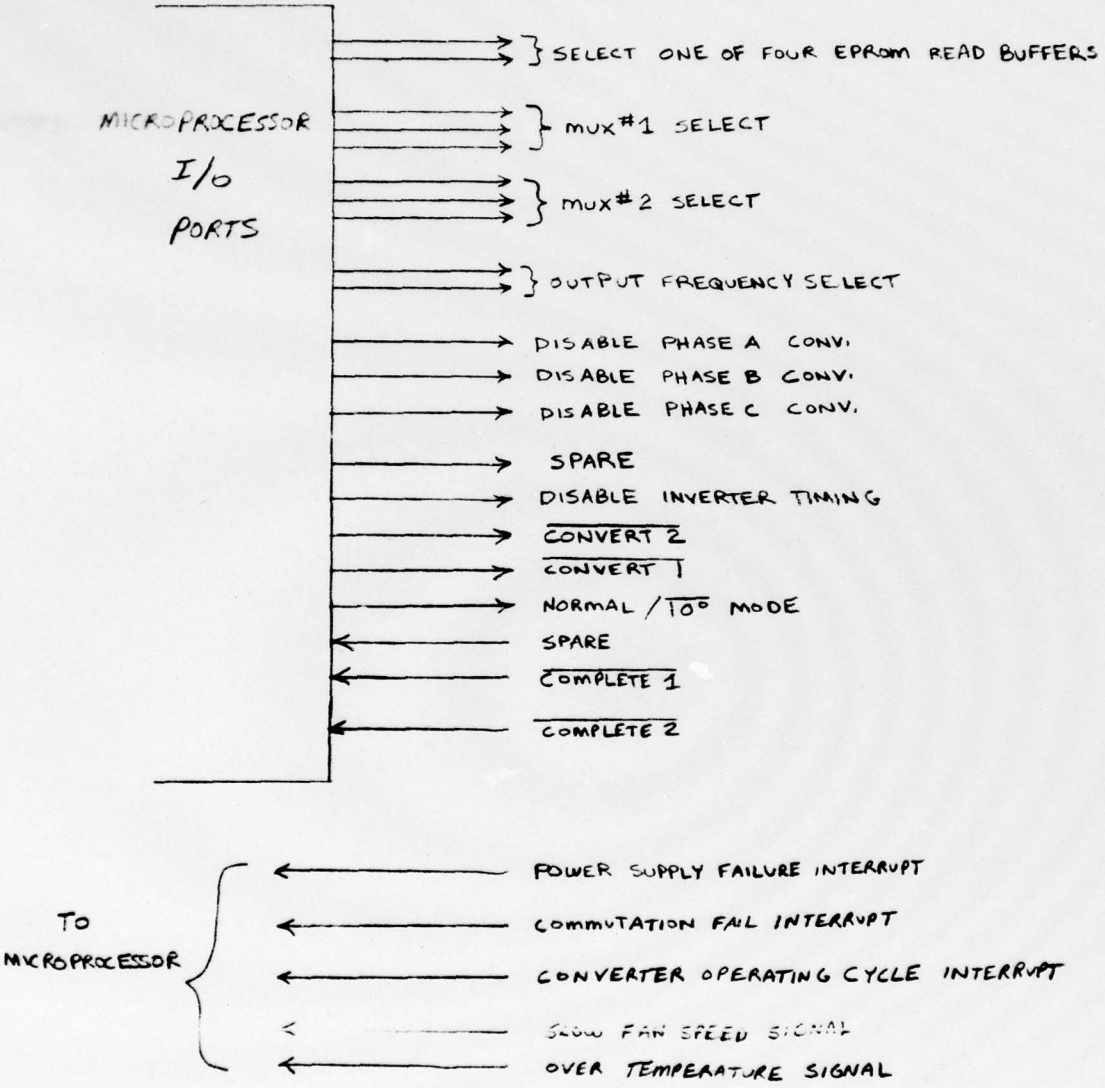


FIGURE 1
I/O SIGNALS

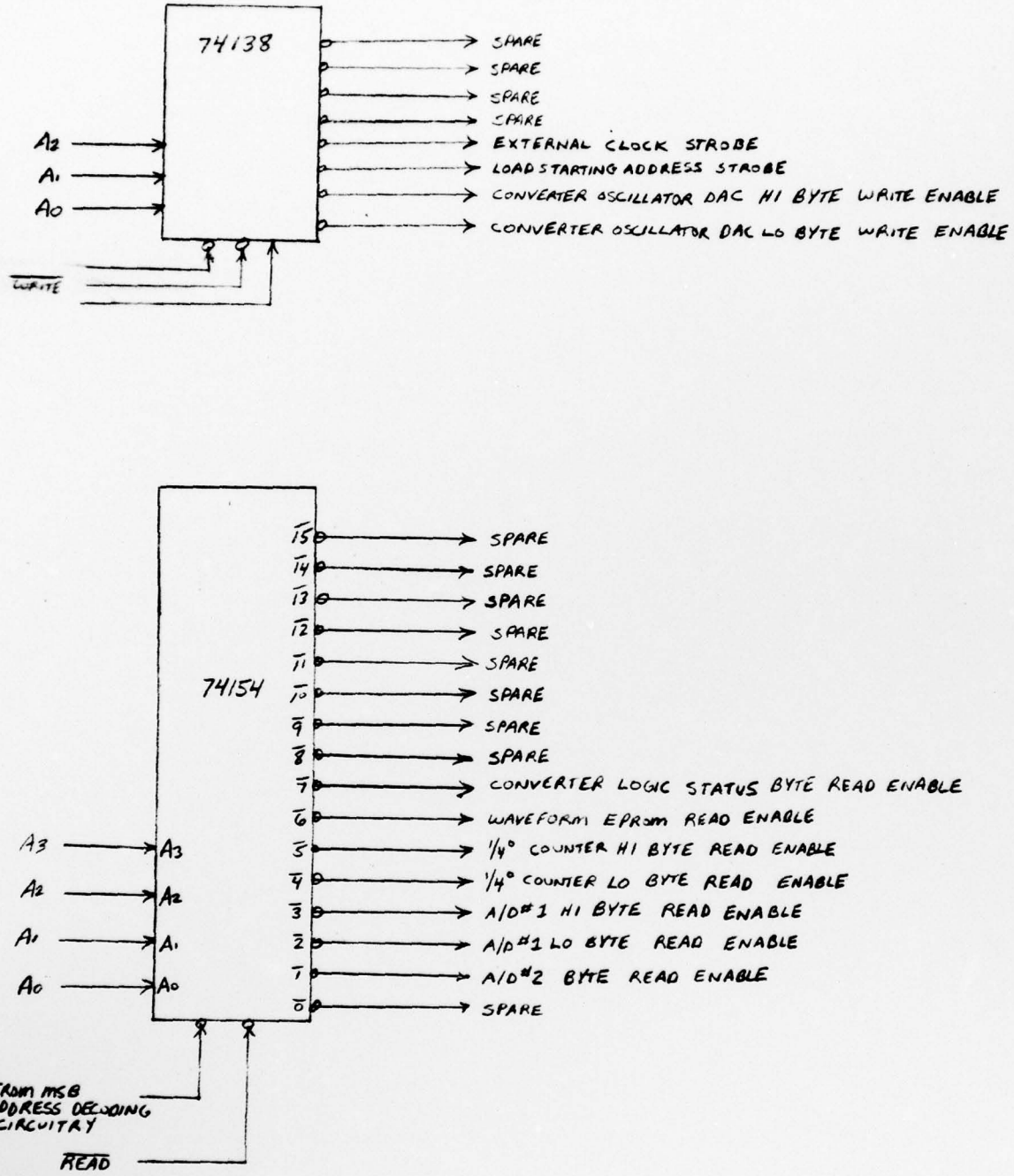


FIGURE 2

DATA BUS READ AND WRITE ENABLE SIGNALS

	Z80A	8085A-2	68B09
MINIMUM SYSTEM			
Chips required	6 or more	3	4
Power supply current	730 ma	530 ma	660 ma
RAM	256 bytes	256 bytes	128 bytes
ROM	2K bytes	2K bytes	2K bytes
Timer/Counter?	Yes	Yes	Yes
Bi-directional I/O lines	32	38	24
ADDRESSING MODES			
Number	10	4	19
8 bit PC relative?	Yes	No	Yes
16 bit PC relative?	No	No	Yes
One byte direct addressing?	limited	No	Yes
One byte direct addressing on any page?	No	No	Yes
Bit addressing?	Yes	No	No
INTERRUPT FEATURES			
Non-maskable interrupt?	Yes	Yes	Yes
Software interrupts?	No	No	Yes
Vectored interrupts to any memory location?	Yes	Yes	Yes
Interrupt that save all registers?	No	No	Yes
Fast interrupt?	Yes	Yes	Yes
INSTRUCTION CYCLE TIME	1µs	.8 µs	1µs

FIGURE #3: COMPARISON BETWEEN Z80A, 8085A-2, & 68B09

		I/O HANDLER	CHAR. SEARCH	COMPUTED GO TO	DOUBLE SHIFT RIGHT 5 BITS	VECTOR ADDITION 16-BIT ELEMENTS	VECTOR ADDITION 8-BIT ELEMENTS	10 X 16 BIT MULTIPLICATION	MOVE BLOCK (64 BYTES)	AVERAGE EXECUTION TIME
6809 (6800)	2.0 MHz	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
	1.5 MHz	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
	1.0 MHz	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Z-80	4.0 MHz	1.4	0.8	2.1	2.7	1.6	1.8	3.3	1.0	1.8
	2.5 MHz	2.2	1.2	3.4	4.4	2.6	2.9	5.2	1.6	2.9
9900	3.0 MHz	2.6	2.3	2.8	1.5	1.7	3.0	0.5	1.6	2.0
6800	2.0 MHz	0.9	1.4	1.9	1.3	3.1	2.8	5.0	3.8	2.4
	1.5 MHz	1.2	1.9	2.5	1.7	4.1	3.7	6.7	4.3	3.3
	1.0 MHz	1.8	2.8	3.7	2.5	6.1	5.5	10.0	6.5	4.9
8080+ (8085A)	3.0 MHz	1.9	1.8	2.8	6.1	2.3	2.7	9.6	2.4	3.7
8085	2.0 MHz	2.8	2.6	4.2	9.1	3.4	4.1	14.3	3.7	5.5

Relative Execution Times For Eight Benchmarks

6809	2.0 MHz	28	287.5	34.5	15	325	180	82	344.5
	1.5 MHz	37.3	383	46	20	433	240	109.3	459.3
	1.0 MHz	56	575	69	30	650	360	164	689
Z-80 (Z-80A)	4.0 MHz	38.3	220.5	73.3	41	518	323	267	342
	2.5 MHz	61.3	352.8	117.2	65.6	828.8	516.8	427.2	547.6
9900	3.0 MHz	72	661	98	22	537	537	42	537
6800	2.0 MHz	24.5	404	64.5	19	993.5	498.5	409.5	1123.5
	1.5 MHz	32.7	539	86.0	25.3	1325	665	546	1498
	1.0 MHz	49	808	129	38	1987	997	819	2247
8080+	3.0 MHz	52.7	506.7	96.7	91.3	732	492	784	841
8085	2.0 MHz	79	760	145	137	1098	738	1176	1262

Actual Execution Times For Eight Benchmarks (μ secs)

MOTOROLA INC.
Integrated Circuits Division
3501 ED BLUESTEIN BOULEVARD
AUST N, TEXAS 78721

ICD 371B (11/77)

TITLE

PART NO. | DWG. NO.

REV. | SHEET 153 OF

FIGURE # 4